

ON THE 10TH ANNIVERSARY OF ULSI WORKSHOP: HISTORY, ANALYSIS, RESEARCHERS

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This is the 10th Anniversary of the International Workshop on Post Binary Ultra-Large-Scale Integration System, so it is time to give a short summary.

There were many questions appearing along with preparing this talk, in particular,

- *In which way the ULSI Workshop influences the International Symposium on Multiple-Valued Logic (ISMVL) and vice versa?*
- *Did this Workshop help researchers?*
- *How has the initial idea by Prof. Kameyama been transformed during 10 years?*
- *Which traditions have been formed in these 10 years?*

With this respect we present our short analysis and hope that it will help to move from this milestone to the next one.



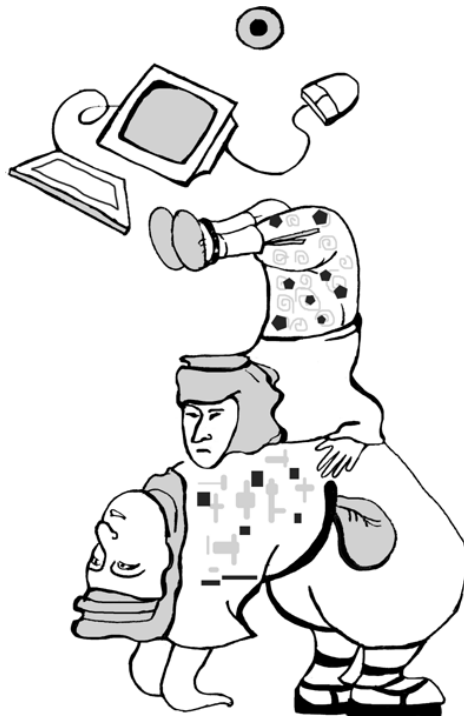
**ULSI Workshop is an event presented on
annual basis since 1992
(vision by designer L. Pottosina)**

1. The first ULSI'1992

The International Workshop on Post-Binary Ultra-Large-Scale Integration Systems (shortly - ULSI Workshop) is an event presented on annual basis since 1992 after or before the ISMVL.

The Chair and Organizer of the first ULSI'1992 Prof. M. Kameyama wrote:

Multiple-valued digital processing is one of the most effective solutions for the problems of design of ultra-large scale integration systems. On the other hand, multiple-valued digital systems have not practically developed in spite of the potential advantages. Why is it so? Because the research cooperations with device, circuit, algorithm, architecture and design levels are not intensively done anywhere. Especially, the interface between devices and systems is most important. In this workshop, we discuss informally such problems so as enhance the research activity for next generation digital systems.



The goal of the first ULSI'1992 Workshop was to establish cooperation between researchers who are developing multiple-valued devices and researchers who are developing algorithms and architectures at the system level (*vision by designer L.Pottosina*)



Researchers visited Japanese Laboratories (*vision by designer L. Pottosina*)

The goal of the first ULSI'1992 Workshop was formulated as follows:

To establish cooperation between researchers who are developing multiple-valued devices and researchers developing algorithms and architectures at the system level. This is motivated by the prospect that the contributions of a group of researches will exceed the contributions of individuals.

29 researchers participated in the first ULSI. They visited Laboratory of Tohoku University (Host T. Higuchi).

2. Analysis

Some traditions have been formed since the first ULSI Workshop. As a rule, ULSI is an one day Workshop (after or before ISMVL). All ULSI Workshops from 1992 to 2001 were supported by different Institutions, including research programs of Japan, France and Poland.

One of the traditions of the Workshop can be formulated as "four friendly NO" that stimulate informal presentation and discussion of a broad range of research topics related to post-binary system design, namely

Four friendly “NO” as the basic principles of ULSI Workshop

- NO reglamentation of topics
- NO reviewing of the submitted papers
- NO requirements for submitted papers, panel materials or oral representation (slides, notes, draft ideas and draws)
- NO registration fees



**The ULSI is an one day Workshop
(after or before IEEE International
Symposium on Multiple-Valued
Logic)
(vision by designer L. Pottosina)**

already. Nine of ten ULSI Workshops were organized by Japanese researchers: two - by M. Kameyama, two - by T. Sasao, one - by T. Sasao and D. Miller, two - by T. Hanyu and two - by T. Waho.

There are many people who founded the basics of the ULSI Workshops. We mention only researchers who played an active role at the first two Workshops. These are *T.Aoki* (Tohoku University, Japan), *J.Butler* (Naval Postgraduate School, USA), *D.Etiemble* (University of Paris, France), *T.Hanyu* (Tohoku University, Japan), *T.Higuchi* (Tohoku University, Japan), *O.Ishizuka* (Miyazaki University, Japan), *S.Karasawa* (Miyagi National College of Tech., Japan), *L.Michel* (Wright Lab, USA), *T.Shibata* (Tohoku

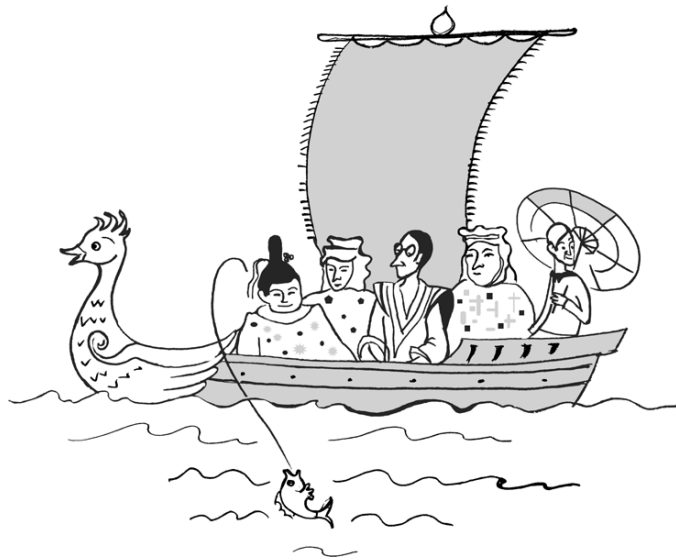
Notice, the idea to prepare a booklet summarizing the presentations belongs to T.Sasao and D.M. Miller who were the Organizers of ULSI in 1996. In the Preface of the ULSI'96 they say: "...*This Booklet is for the benefit of attendees at the Workshop and is not intended for distribution beyond that forum.*" The organizers of the next Workshops supported this idea, so all researchers who attended ULSI in 1996-2000 had the Extended Abstracts.

In Table 1 we indicate 10 ULSI and 10 ISMVL from 1992 to 2001. The question is: Which goal we try to analyze the talks with (Table 2). This is the base for deeper analysis. As we see, the Organizers of Workshops try to keep the "red line" of the initial idea as "Technology, device and system innovations" in different ways. Table 3 helps us to analyze the efforts of the Organizers in detail.

3. Organizers of ULSI

Initiated by Prof. Kameyama in 1992, the ULSI Workshop has been held for 10 years

University, Japan), C.B.Silio (University of Maryland, USA), K.C.Smith (University of Toronto, Canada), A.Taddiken (Texas Instruments Inc., USA), N.Takagi (Toyama University, Japan), T.Tanoue (Hitachi Ltd, Japan).



ULSI has been organized by M. Kameyama, T. Sasao, D. Miller, T. Hanyu and T. Waho (vision by designer L. Pottosina)



Future of the ULSI Workshop (vision by designer L. Pottosina)

4. Future

We asked some researchers to answer two questions:

- In which way non-formal discussions through ULSI Workshops help you to solve your own research problems?
- In which way do you see the evolution of the ULSI?

Some of answers are given in Table 4.

Acknowledgements

We express our gratitude to Prof. M. Kameyama (Japan), Prof. T.Sasao (Japan), Prof. R. Stankovic (Yugoslavia), Prof. C. Moraga (Germany), Prof. M. Perkowski (USA) and Prof. J. Butler (USA).

We asked designer Dr L. Pottosina give her vision of ULSI Workshops based on our paper. She has sent us six ironic pictures to illustrate the paper.

References

1. Extended Abstracts ULSI'96-ULSI'2000
2. ULSI'94-95 Archive by Prof. M. Kameyama
3. ULSI'94-95 Archive by Prof. R. Stankovic
4. ULSI'94-95 Archive by Prof. J. Butler

Table 1

Ten years of ISMVL + ULSI: 1992-2001

Year	ISMVL	ULSI	Place	Chair
1992	The 22-nd	The 1-st	Tohoku University, Sendai, Japan	Michitaka Kameyama (<i>Tohoku University, Japan</i>)
1993	The 23-rd	The 2-nd	Sacramento, USA	Michitaka Kameyama (<i>Tohoku University, Japan</i>)
1994	The 24-th	The 3-rd	Boston, Massachusetts, USA	Tsutomu Sasao (<i>Kyushu Institute of Technology, Iizuka, Japan</i>)
1995	The 25-th	The 4-th	Indiana University Bloomington, Indiana, USA	Tsutomu Sasao (<i>Kyushu Institute of Technology, Iizuka, Japan</i>)
1996	The 26-th	The 5-th	University of Santiago de Compostela, Spain	Tsutomu Sasao (<i>Kyushu Institute of Technology, Iizuka, Japan</i>), D. Michael Miller (<i>University of Victoria, Canada</i>)
1997	The 27-th	The 6-th	St. Francis Xavier University, Antigonish, Nova Scotia, Canada	Takahiro Hanyu (<i>Tohoku University, Japan</i>)
1998	The 28-th	The 7-th	Fukuoka Software Research Park, Fukuoka, Japan	Takahiro Hanyu (<i>Tohoku University, Japan</i>)
1999	The 29-th	The 8-th	Albert-Ludwigs University, Freiburg im Bresgau, Germany	Takao Waho (<i>Sophia University, Tokyo, Japan</i>)
2000	The 30-th	The 9-th	Portland State University, Oregon, USA	Takao Waho (<i>Sophia University, Tokyo, Japan</i>)
2001	The 31-st	The 10-th	Polish Academy of Sciences, Warsaw, Poland	Vlad Shmerko (<i>Technical University of Szczecin, Poland/ State University of Informatics and Radioelectronics, Belarus</i>)

Table 2**Hot talks at ULSI 1992-2001**

1992	<ul style="list-style-type: none"> • Device innovation • System innovation 	Sendai, Japan
1993	<ul style="list-style-type: none"> • System and implementation • Large-scale design methodology for ULSI systems • Application of ULSI systems 	Sacramento, USA
1994	<ul style="list-style-type: none"> • Systems and Implementation • Digital Field Programmable Arrays and Systems • Analog Field Programmable Arrays and Systems 	Boston, Massachusetts USA
1995	<ul style="list-style-type: none"> • Novel Computation • Logic Design 	Indiana University, Bloomington, USA
1996	<ul style="list-style-type: none"> • Decision diagrams • Architectural and nano-electronics strategies for 2D and 3D ULSI signal processing 	Santiago de Compostela, Spain
1997	<ul style="list-style-type: none"> • Minimization of incompletely specified logic functions • Feedback in combinational logic circuits • Fuzzy logic and its applications • Challenges of multiple-valued VLSI circuits and devices 	Antigonish, Canada
1998	<ul style="list-style-type: none"> • Gr.C.Moisil and his school in algebraic logic, • Boolean design and autodual negative gates • Challenges of multiple-valued VLSI circuits and devices • BDDs/MDDs • Testing in multiple-valued logic networks 	Fukuoka Software Research Park, Fukuoka, Japan
1999	<ul style="list-style-type: none"> • Intelligent integrated systems architecture • Nanoelectronics • Decision diagrams • Information theory to logic design 	Freiburg-im- Bresgau, Germany
2000	<ul style="list-style-type: none"> • Algorithms and Logic Design • LSI circuits and devices 	Portland, USA
2001	<ul style="list-style-type: none"> • Concept of flexibility in logic design • Formal methods in VLSI CAD • Reversible and quantum logic • Komamiya equation, linear decision diagrams 	Warsaw, Poland

Table 3:

**History of International Workshops on Post-Binary ULSI Systems,
1992-2001**

<p>The 1-st ULSI-1992</p> <p style="text-align: center;">Tohoku University, Japan</p> <p>Part 1. Device innovation: <i>neuron MOS transistor, multi-step function, MOS transistor, quantum device, biochip</i></p> <p>Part II. System innovation: <i>logic design, circuit design, CAD tools for MVL, communication applications, AI applications</i></p> <p>Panel discussion (Chair J.Butler, USA)</p>	<p>Chair: M. Kameyama</p>
<p>The 2-nd ULSI-1993</p> <p style="text-align: center;">Sacramento, USA</p> <p>Part I. System and Implementation: <i>prospects of nanoelectronic circuits in deep submicron age, prospects of future high-integration circuit technology, device-model-based post-binary electronic systems</i></p> <p>Part II. Large-scale design methodology for ULSI systems: <i>recent development of logic design methodology, next generation CAD tool for ULSI systems, highly parallel logic design for ultra-high-speed ULSI processors</i></p> <p>Part III. Application of ULSI systems: <i>real-time applications in ULSI systems, neural and fuzzy network applications using multiple-valued logic, artificial intelligence using multiple-valued logic</i></p>	<p>Chair: M. Kameyama</p>
<p>The 3-rd ULSI-1994</p> <p style="text-align: center;">Boston, Massachusetts, USA</p> <p>PART I: Systems and Implementation (Organizer: Lutz Micheel, USA): <i>Rule-Programmable Multiple-Valued Matching VLSI Processor for Real-Time Rule-Based Systems; Advanced System Architecture and Nanoelectronics; Ultra Fast; Ultra Dense Circuits Based on Sidewall RHETs, RTDs, and 3-D Integrated Loads</i></p> <p>PART II: Digital Field Programmable Arrays and Systems (Organizer: M.Perkowski, USA): <i>Field Programmable Gate Arrays, The Technology; Physical Design and Logic Synthesis; Design Automation for FPGAs, An Overview</i></p> <p>PART III: Analog Field Programmable Arrays and Systems (Organizers: G.Gulak, Canada, and M.Perkowski, USA) : <i>Field Programmable Analog Devices; On the decomposition of continuous functions</i></p> <p>PART IV: Intelligent Systems (Organizer: T.Hanyu, Japan): <i>The Role of Continuous-Valued Logic in a Mobile Robot; Super Intelligent Vehicles; Application to Multiple-Valued Intelligent Integrated Systems</i></p>	<p>Chair: T. Sasao</p>

Table 3: Continuation

<p>The 4-th ULSI-1995 Indiana University Bloomington, Indiana, USA Session I: Novel Computation (Chair J. Mills, USA): <i>Thermodynamics of Computation and Complexity, Information Theory of Lukasiewicz Logic Arrays</i> Session II: Logic Design (Chair T.Sasao, Japan): <i>Ordered Kronecker Function Decision Diagrams. On a design of AND-OR-EXOR logic circuits. Design of High Performance Digital System Based on Linearity</i></p>	<p>Chair: T. Sasao</p>
<p>The 5-th ULSI-1996 Santiago de Compostela, Spain Invited talk: R. Drechsler, <i>Extensions of decision diagrams to the word-level</i> Contributed presentation: <i>Complex Hadamard decision diagrams, Fourier decision diagrams on finite non-Abelian groups in optimization, on using decision diagrams to compute logic and arithmetic polynomial forms for incompletely specified MVL functions, exact minimization of networks with complex gates using terminal suppressed binary decision diagrams and dissected pairs, using decision diagrams to design ULM for FPGAs, a note on symbolic simulation using decision diagrams</i> Panel session (Organizer Lutz J. Micheel): <i>architectural and nano-electronics strategies for 2D and 3D ULSI signal processing</i></p>	<p>Chair: T. Sasao and D. M. Miller</p>
<p>The 6-th ULSI-1997 Antigonish, Nova Scotia, Canada Tutorial session (Chair T. Hanyu, Japan): <i>Completeness, composition and clones in multiple-valued logics, fuzzy logic and its mathematical properties, multiple-valued logic design, multiple-valued VLSI circuits and systems</i> Session I. Minimization of incompletely specified logic functions (Chair V.Shmerko, Poland/Belarus): <i>hardware realization to minimize incompletely specified functions, minimization of partially mixed polarity Reed-Muller expansions, on feasible transforms for incompletely specified functions, efficient algorithm for minimization of polynomial representations of weakly specified Boolean functions and systems, parallel and distributed realization of irredundant minimization of MVL functions, optimizing the calculation of logic derivatives through decision diagrams, feedback in combinational logic circuits</i> Session II. Fuzzy logic and its applications (Chair Y. Hata, Japan): <i>On the computational power of continuous dynamical systems, fuzzy optimization of industrial power plants, fuzzy medical image processing</i> Session III. Challenges of multiple-valued VLSI circuits and devices (Chair K.S. Smith, Hong-Kong): <i>new architecture for multiple-valued VLSI systems, beyond-binary arithmetic, multi-valued ferroelectric associative memory design, MVL circuits with quantum devices</i></p>	<p>Chair: T. Hanyu</p>

Table 3: Continuation

<p>The 7-th ULSI-1998</p> <p>Kyushu Institute of Technology, Iizuka, Japan</p> <p>Tutorial session (Chair D. Simovici, USA): Gr.C.Moisil and his school in algebraic logic, Boolean design and autodual negative gates</p> <p>Session I. Challenges of multiple-valued VLSI circuits and devices (Chair T. Hanyu, Japan): <i>10-GHz multiple-valued circuits using resonant-tunneling devices; CMOS field-programmable analog and mixed signal arrays; a mixed sensor, analog and digital architecture for a post-binary system LSI; wave parallel computing paradigm based on multiplexing of signals</i></p> <p>Session II. BDDs / MDDs (Chairs T. Sasao, Japan, and R. Drechsler, Germany): <i>efficient methods for a simple disjoint decomposition and a non-disjoint bi-decomposition; improving the efficiency of symbolic FSM traversal by dynamic removal of flip-flops; an exponential lower bound on the size of a binary moment diagram representing division; word-level decision diagrams in verification; on dependable strategy for dynamic reordering algorithms</i></p> <p>Session III. Testing in multiple-valued logic networks (Chair V.Shmerko, Poland / Belarus): <i>minimal universal test set for a single faults in Galois-sum-of-products circuits; multiple-valued combinational circuits synthesised by evolvable hardware approach; some new results of experiments on testing MVL combinational circuits with generalized D-algorithm; four remarks on minimization of strongly unspecified logic functions; genetic test pattern generation for MVL combinational circuits</i></p>	<p>Chair: T. Hanyu</p>
<p>The 8-th ULSI-1999</p> <p>Freiburg-im-Bresgau, Germany</p> <p>Invited talks: M. Kameyama, <i>Innovation of intelligent integrated systems architecture - future challenge.</i> H. L. Hartnagel, <i>Quantum electronic circuit concepts by nanometric technology</i></p> <p>Session I. Nanoelectronics: <i>high-speed single-electron memory and logic, programmable HBT-quantum dot structure for arithmetic MVL, GaAs- and InP-based technologies of resonant tunneling devices, nano-fabrication technology and silicon nano-devices</i></p> <p>Session II. BDD/MDD: <i>Nonapproximability results for OBDD- and FBDD-minimization, Improving reachability analysis by means of activity profiles, word-level verification of data-path operations, interval diagram techniques and their applications</i></p> <p>Session III. Application of information theory to logic design (Chair: S. Yanushkevich, Poland/Belarus): <i>information theory approach in logic design: results, trends and non-solved problems, some remarks on information entropy, vitality and information engine, information theoretical approach in evolutionary circuit design, information theoretical approach in Reed-Muller expansion minimization</i></p>	<p>Chair: T. Waho</p>

Table 3: Continuation

<p>The 9-th ULSI-2000</p> <p style="text-align: center;">Portland, Oregon, USA</p> <p>Session I.</p> <p>Algorithms and Logic Design: <i>beyond-binary arithmetic – algorithms and implementation, multiple-valued threshold logic: past, present and future, disjoint Bi-decomposition of Boolean functions in the Walsh spectral domain</i></p> <p>Session II.</p> <p>LSI circuits and devices: <i>multiple-valued logic-in-memory VLSI and its application, development of negative differential resistance devices for multiple-valued circuit application, design of multiple-valued logic circuits using neuron-MOS transistors</i></p>	<p>Chair: T. Waho</p>
<p>The 10-th ULSI-2001</p> <p style="text-align: center;">Warsaw, Poland</p> <p>Opening talk: ON THE 10TH ANNIVERSARY OF ULSI WORKSHOP: HISTORY, ANALYSIS, RESEARCHERS</p> <p>Invited talks:</p> <ul style="list-style-type: none"> • H. Sawada, S. Yamashita, A. Nagoya (<i>NTT, Japan</i>) SPFD: A METHOD TO EXPRESS FUNCTIONAL FLEXIBILITY • T. Luba, M. Rawski (<i>Poland</i>) FUNCTIONAL DECOMPOSITION - THE VALUE AND IMPLICATION FOR BOTH DIGITAL DESIGNING AND DATA ANALYSIS • M.Perkowski, A. Al-Rabadi (<i>USA</i>), P. Kerntopf (<i>Poland</i>), A. Mishchenko, M. Chrzanowska-Jeske (<i>USA</i>), THREE – DIMENSIONAL REALIZATION OF MULTIPLE-VALUED FUNCTIONS USING REVERSIBLE LOGIC • R. S. Stankovic(<i>Yugoslavia</i>), T. Sasao (<i>Japan</i>) KOMAMIYA EQUATION FOR MULTIPLE-VALUED ADDERS <p>Session I. Formal methods in VLSI CAD (<i>Chair F. Schmiedle</i>)</p> <p>Session II. Reversible and Quantum Logic (<i>Chair M. Perkowski</i>)</p> <p>Session III. To the honor of pioneering results by Y. Komamiya (<i>Chair T. Sasao</i>)</p>	<p>Chair: V, Shmerko</p>

Table 4

Towards ULSI Workshop in New Millenium

<p>Question: <i>In which way has ever a non-formal discussion through ULSI Workshops helped you to solve your own research problems?</i></p>	<p>Question: <i>In which way do you see the evolution of the Workshop?</i></p>
<p>Prof. M. Perkowski (Portland State University, OR, USA)</p>	
<p>I had many discussions with ULSI participants in the past. Particularly, the discussion about the Linearly Independent Logic and non-singularity Prof. Stankovic, which helped both of us to clarify important issues related to transforms, expansions and diagrams. I learned a lot from papers of Profs. Kameyama, Higuchi, Hanyu and Aoki. I talked to them a lot to learn about their ideas on the intersection of system, logic and physical design. This group, in contrast to many other researchers, has a continued definite research direction, and their contributions are consistent in building real ULSI systems. Talking to them helped me to formulate better and deeper research problems in logic synthesis for future technologies and see things broader. Many discussions with Prof. Sasao on exor logic and its generalizations, as well as decomposition helped me to understand better his research ideas. I found the general concept of systematic analysis of using information theory to logic synthesis advocated by Profs. Shmerko and Yanushkevich quite interesting. I found also interest in test and verification of multi-valued logic circuits as presented at the workshop, and especially I talked to Dr. Dubrova about Galois logic. She helped me to generalize some of my results and find literature. Discussions with her were always very useful to me. Professor Moraga has been always an non-exhaustable source of new</p>	<p>I can understand this question in two ways: a) how the workshop did evolve? b) how I wish the workshop to evolve? Answering variant a): I would say that the Workshop did not find its own specifics and research niche. It only reflected the interests of researchers in multiple-valued logic. Together with ISMVL, workshop evolved towards decision diagrams (multi-valued and other) and their applications and modern circuit realization techniques. Because there have been very few participants - researchers who actually build systems, there have been very few papers about actual issues of designing systems-on-a-chip. In my opinion we should invite more researchers who work in the areas of system design, multimedia processing, new realization technologies, intellectual property chips, digital signal processing and/or robotics to present the real issues of designing ULSI chips. So far, the leading researches in this area has been from Profs. Higuchi's and Kameyama's group who have practical experience of designing non-binary large chips. The nanotechnology papers from industry were very enlightning, but in my opinion too much separated from the mainstream of the interests of this workshop. We need more papers that would bridge the gap between nano-technologies such as quantum or bio-computing and the mainstream of synthesis methods. There was notable lack of papers in layout and physical design, and also very few papers in system design issues. These are also issues of high interest to future ULSI and should be addressed. Especially physical design for new technologies is now of the highest importance to IC companies, and these issues have been never to my recollections addressed in ULSI symposium. (with exception of papers by Chrzanowska-Jeske and Marek Perkowski in 1994). Answering variant b): The main weakness of the workshop has been a very low participation of researchers from industry and practicing engineers. This caused on one hand that issues were</p>

<p>information and ideas in Genetic Algorithms, spectral methods and many other. The atmosphere of non-competitive exchange of research results, which is typical for mathematics and logic conferences but is non-existent in competitive US electronics conferences, is a VERY, VERY important asset of both ISMVL and ULSI, which should be preserved and enhanced.</p>	<p>discussed that are too academic and not really related to the future ULSI technologies, and on the other hand several top practical issues of designing ULSI chips were not discussed at all. I would suggest to have a panel discussion which would attempt at creating an outline of future researches with clearly defined goals. This workshop results should be more visible in international CAD and System-on-a-chip communities, through journal papers, presentations on world congresses and books. Workshop should go towards logic synthesis, physical design and system design using new technologies such as reversible logic, quantum logic, bio-computing and optical computing. It should find its own unique identity.</p>
<p>Prof. M. Kameyama (Tohoku University, Japan)</p>	
	<p>Device innovation such as multiple-valued quantum devices encouraged us to develop a new system architecture. The important thing is that the Workshop gives us new dreams, and gives us a hint for a new concept.</p>
<p>Prof. C. Moraga (Dortmund University, Germany)</p>	
<p>Your official questions are difficult, since I would have to answer "none" to the first one. Indeed no ULSI-talk has helped me to solve an own research problem; however I have heard quite motivating talks, very encouraging to keep on doing research. For instance, every talk on the latest advances in hardware (devices) is a motivation for me to keep on working on better design methods. And this is already very valuable</p>	<p>I think this is the main achievement of the ULSI-series: to offer a possibility of discussing advanced subjects that are not necessarily in the core of MV, but that may broaden our horizons or open new roads of research.</p>
<p>Prof. S. Yanushkevich (Technical University of Szczecin, Poland)</p>	
<p>Basing on my experience, I can say that the Workshop is a great chance for researchers who start in the area, to acquaint themselves with the state-of-the-art in the post-binary systems and applications, that they never cannot be aware of the journal publications neither conference because of long processing cycle.</p>	<p>It should be turned back to the initial idea formulated by Prof. M. Kameyama: <i>"To establish cooperation between researchers who are developing multiple-valued devices and researchers who are developing algorithms and architectures at the system level."</i></p>